EL977166548US

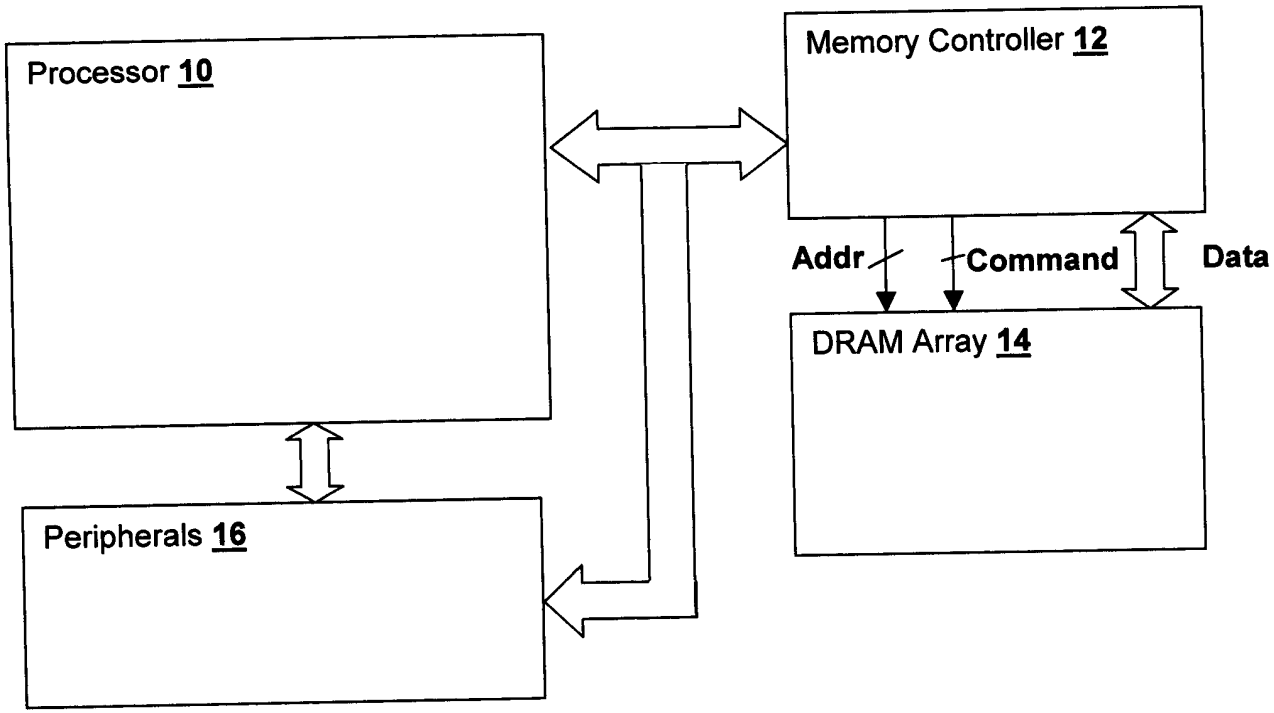


Fig. 1

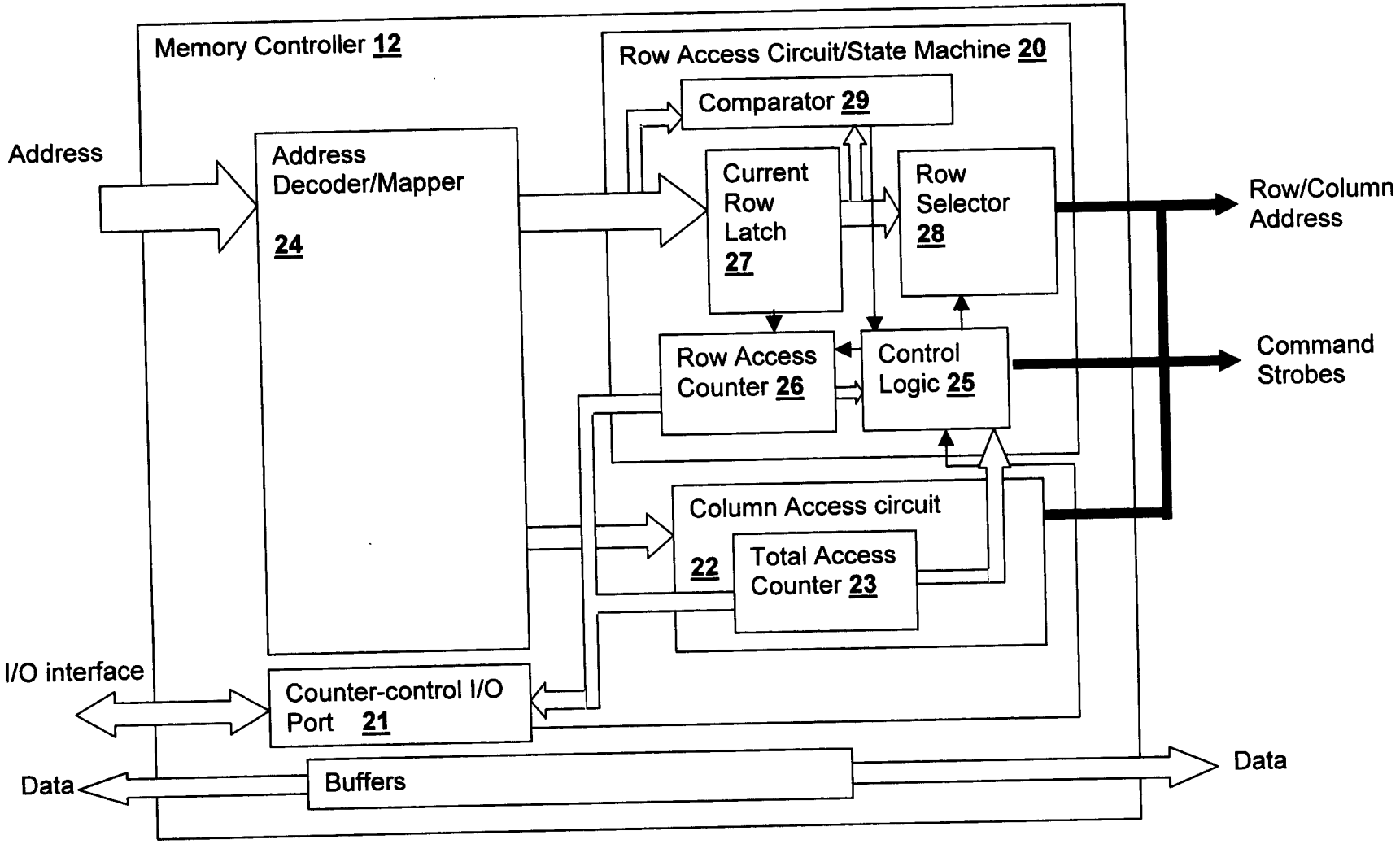

Memory Controller 12
Row Access Circuit/State Machine 20
Comparator 29
Address
Address Decoder/Mapper
24
Current Row Latch 27
Row Selector 28
Row/Column Address
Row Access Counter 26
Control Logic 25
Command Strobes
Column Access circuit
22
Total Access Counter 23
I/O interface
Counter-control I/O Port 21
Data
Buffers
Data

Fig. 2

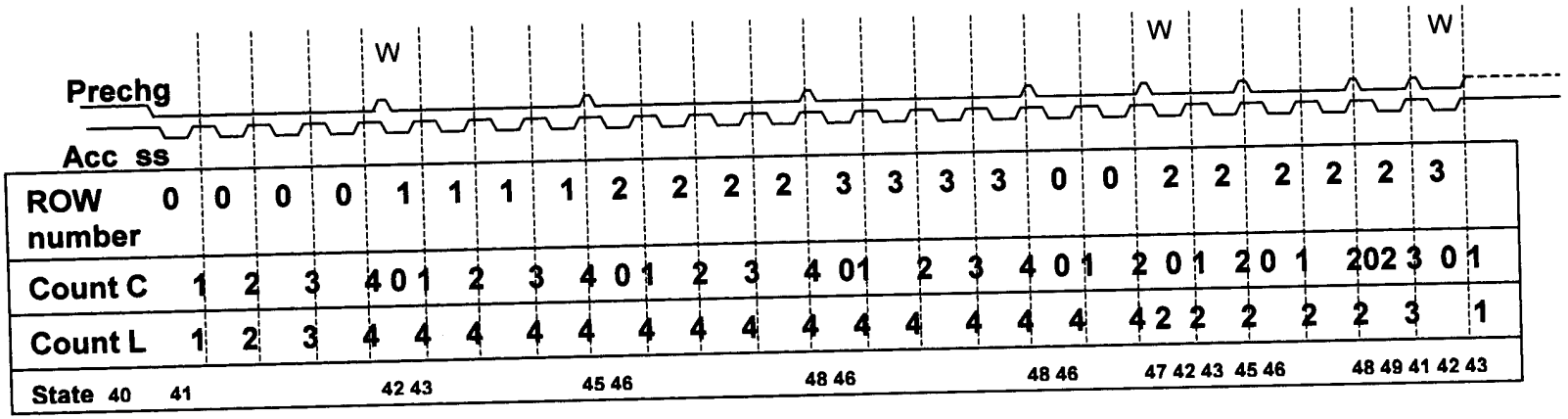
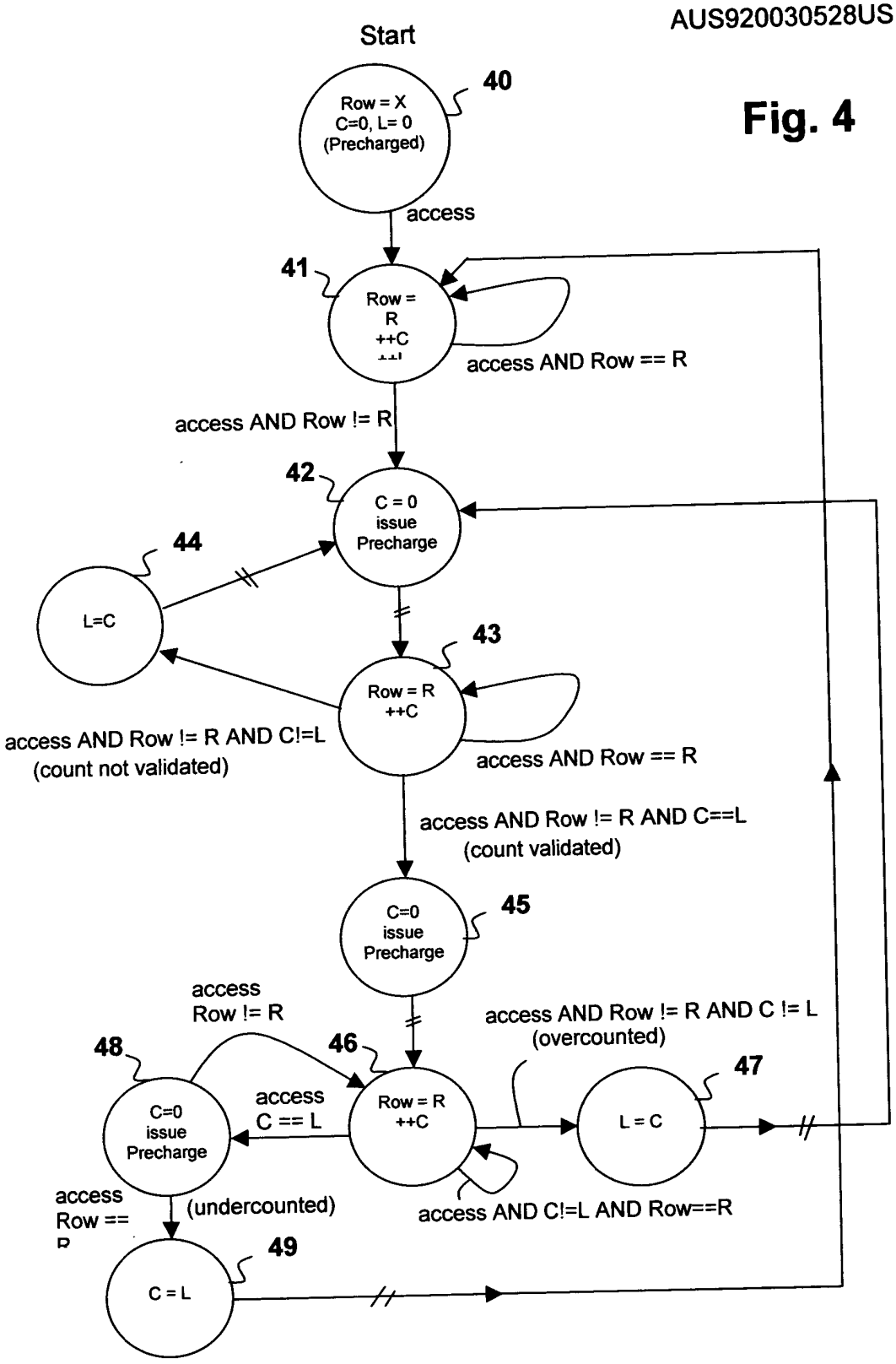

W
W
W
Prechg
Acc ss
ROW number 0 0 0 0 1 1 1 1 2 2 2 2 3 3 3 3 0 0 2 2 2 2 2 3
Count C 1 2 3 4 0 1 2 3 4 0 1 2 3 4 01 2 3 4 0 1 2 0 1 2 0 1 202 3 0 1
Count L 1 2 3 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 2 2 2 2 2 3 1
State 40 41 42 43 45 46 48 46 48 46 47 42 43 45 46 48 49 41 42 43

Fig. 3

Fig. 4


Start
40
Row = X
C=0, L= 0
(Precharged)
access
41
Row =
R
++C
access AND Row == R
access AND Row != R
42
C = 0
issue
Precharge
44
L=C
43
Row = R
++C
access AND Row != R AND C!=L
(count not validated)
access AND Row == R
access AND Row != R AND C==L
(count validated)
C=0
issue
Precharge
45
access
Row != R
access AND Row != R AND C != L
(overcounted)
48
46
47
C=0
issue
Precharge
access
C == L
Row = R
++C
L = C
access
Row ==
R
(undercounted)
access AND C!=L AND Row==R
49
C = L